a silicon film being formed on walls closer to said gate electrode to be connected with said gate electrode, a surface of said silicon film, together with said gate electrode being silicified and forming a concave portion.

12. (Amended) A MIS transistor including:

a silicon substrate having a main surface;

a gate electrode being formed to be opposed to said main surface through a gate insulating film and having a silicified portion at an opposite side of said gate insulating film;

side walls being formed on said main surface on both sides of said gate electrode, and having L-shaped sections being higher than said silicified portion; and

impurity regions formed inside said main surface to be opposed to said gate electrode in regard to said side walls, each of said impurity regions having a silicified surface.

REMARKS

Favorable reconsideration of this application, in view of the following comments and as presently amended, is respectfully requested.

Claims 10-13 are pending in this application. Claim 10 was rejected under 35 U.S.C. § 102(e) as anticipated by U.S. patent 5,776,822 to Fujii et al. (herein "Fujii"). Claim 12 was rejected under 35 U.S.C. § 102(e) as anticipated by U.S. patent 5,702,986 to Mathews et al. (herein "Mathews"). Claim 11 was rejected under 35 U.S.C. § 103(a) as unpatentable over Fujii in view of U.S. patent 5,554,566 to Lur et al. (herein "Lur"). Claim 13 was rejected under 35 U.S.C. § 103(a) as unpatentable over Mathews in view of Lur.

Addressing first the rejection of Claim 10 under 35 U.S.C. § 102(e) as anticipated by Fujii, and the further rejection of Claim 11 under 35 U.S.C. § 103(a) as unpatentable over Fujii in view of Lur, those rejections are traversed by the present response.

It is initially noted that Claim 10 is amended by the present response to clarify features recited therein. Claim 10 more clearly recites that a surface of the silicon film, together with the gate electrode, are "silicified" and "forming a concave portion".

In contrast to the features now recited in Claim 10, in Fujii the silicide film 135 does not form a concave portion, and thus fails to meet the limitations of amended Claim 10.

It is also noted that no teachings in Lur were relied upon in the rejection to Claim 10.

In such ways, independent Claim 10, and Claim 11 dependent therefrom, are believed to patentably distinguish over the teachings in Fujii, and the further rejection based on Lur.

Addressing now the rejection of Claim 12 under 35 U.S.C. § 102(e) as anticipated by Mathews, and the further rejection of Claim 13 under 35 U.S.C. § 103(a) as unpatentable over Mathews in view of Lur, those rejections are also traversed by the present response.

Initially, it is noted that Claim 12 is amended by the present response to clarify subject matter recited therein. The subject matter of Claim 12 is supported, as one example, in Figure 42 of the present specification. According to Claim 12 "impurity regions" are formed inside of a main surface opposed to a gate electrode in regard to sidewalls, and "each of said impurity regions having a silicified surface".

In contrast to Claim 12, in Mathews the surface of the polycrystalline silicon layer 11 to become a gate electrode is silicified to provide layer 12 before doping source/drain impurities. As a result, in Mathews there can clearly be no incentive or motivation to silicify the surface of impurity layers 23 and 24, in contrast to the requirements of the "impurity regions" recited in amended independent Claim 12.

In such ways, amended independent Claim 12 patentably distinguishes over the teachings in Mathews.

Moreover, no teachings in Lur were relied upon with respect to the rejection of independent Claim 12, and in such ways independent Claim 12, and Claim 13 dependent therefrom, are believed to patentably distinguish over the teachings in Mathews, and the further rejection in view of Lur.

As no other issues are pending in this application, it is respectfully submitted that the present application is now in condition for allowance, and it is hereby respectfully requested that this case be passed to issue.

Respectfully submitted,

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IN THE CLAIMS

Please amend Claims 10 and 12 to read as follows:

--10. (Amended) A MIS transistor including:

a gate electrode being formed to be opposed to a silicon substrate through a gate insulating film [and having a silicified upper portion]; [and]

side walls being formed on said silicon substrate on both sides of said gate electrode, said side walls being higher than said gate electrode[,]; and

[said side walls being provided with] a silicon [films] film being formed on walls closer to said gate electrode to be connected with said gate electrode, a surface of said silicon film, together with said gate electrode being silicified [up to surfaces of said silicon films] and forming a concave portion.

12. (Amended) A MIS transistor including:

a silicon substrate having a main surface;

a gate electrode being formed to be opposed to [a silicon substrate] said main surface through a gate insulating film and having a silicified [upper] portion at an opposite side of said gate insulating film; [and]

side walls [having L-shaped sections] being formed on said [silicon substrate] main surface on both sides of said gate electrode, [said side walls] and having L-shaped sections being higher than said [gate electrode] silicified portion; and

impurity regions formed inside said main surface to be opposed to said gate electrode in regard to said side walls, each of said impurity regions having a silicified surface.--